REMARKS

The present application was filed on September 30, 2003 with claims 1-20.

Claims 6, 10, 11, and 15 are objected to due to alleged informalities.

Claims 1, 19, and 20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

Claim 20 is rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,872,770 (hereinafter Park).

With regard to the §112 rejection of claims 1, 19 and 20, Applicant has amended the claims without prejudice to replace the objected-to recitations of "the performance" with "performance" so as to overcome the alleged antecedent basis issues and thus expedite prosecution.

With regard to the objections to claims 6, 10, 11 and 15, Applicant has amended these claims without prejudice in a manner believed to overcome the objections and thus expedite prosecution.

With regard to the §101 rejection of claim 20, Applicant respectfully submits that an article of manufacture comprising a machine-readable storage medium having program code stored thereon for use in a processor, wherein the program code when executed in the processor implements one or more steps producing a concrete, useful, and tangible result constitutes a proper claim of statutory subject matter. See, e.g., In re Beauregard, 53 F.3d 1583; 35 USPQ2d 1383 (Fed. Cir. 1995); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Notwithstanding the traversal, Applicant has amended independent claim 20 without prejudice solely in order to expedite prosecution.

Claim 1 is directed to a processor comprising controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor and memory circuitry comprising a continuity check cache. The continuity check cache stores an identifier for each of a subset of the plurality of flows. The controller circuitry controls access to a set of continuity check counters comprising a counter for each of the plurality of flows.

The controller circuitry determines if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check cache. If the given flow has such an entry, the controller circuitry prevents a corresponding one of the continuity check counters from being updated. If the given flow does not have such an entry, the controller circuitry clears the corresponding one of the continuity check counters and stores a flow identifier for the given flow in the continuity check cache.

It is important to note that claim 1 specifies that whereas the set of continuity check counters comprises a counter for each of the plurality of flows, the continuity check cache stores an identifier for each of a subset of the plurality of flows. Thus, it is inherent in claim 1 that the number of flows for which the continuity check cache stores an identifier is less than number of counters within the set of continuity check counters.

The Examiner argues that the above-noted limitations of claim 1 are met by the arrangement shown in FIG. 3 of Park, except in so far as Park fails to disclose memory circuitry implemented as a continuity check cache. Specifically, the Examiner argues that the recited set of continuity check counters comprising a counter for each of the plurality of flows is met by the continuity clock timer part 32.

The Examiner contends that the limitation of claim 1 wherein memory circuitry storing an identifier for each of a subset of the plurality of flows is disclosed by Park at column 9, lines 1-12. Applicant notes that column 9, lines 5-8, discloses that "continuity check cell/user cell comparator 31 compares the received channel identifiers VPI/VCI with channel identifiers VPI/VCI of active connections from the continuity check channel cell registration part 34" and that, moreover, Park at column 9, lines 57-60, teaches that the "continuity check cell registration part 34 is adapted to store therein . . . channel identifiers of continuity check connections." Accordingly, it appears that the Examiner is arguing that continuity check cell registration part 34 corresponds to the recited memory circuitry comprising a continuity check cache, which stores an identifier for each of a subset of the plurality of flows.

However, in contrast to the claimed arrangement wherein the number of flows for which the continuity check cache stores an identifier is less than number of counters within the set of continuity

check counters, Park teaches at column 9, lines 23-26, that the "continuity clock timer part 32 includes a plurality of timers corresponding respectively to continuity check connections in the continuity check cell channel registration part 34." See also FIG. 3 of Park, which shows continuity check timer part 32 comprising Timer-1, Timer-2, ..., Timer-N, and continuity check channel registration part 34 comprising Continuity Checking Cell Channel-1, Continuity Checking Cell Channel-2, ..., Continuity Checking Cell Channel-N.

Accordingly, Park not only fails to suggest the claimed arrangement wherein a set of continuity check counters comprises a counter for each of the plurality of flows and a continuity check cache stores an identifier for each of a subset of the plurality of flows, but in fact teaches away by instead disclosing an arrangement wherein "continuity clock timer part 32 includes a plurality of timers corresponding relatively to continuity check connections in the continuity check cell channel registration part 34."

Moreover, even if Park were to be modified in the manner suggested by the Examiner in the present Office Action at page 5, second paragraph, i.e., by implementing the continuity memory disclosed at column 9, lines 1-12, as fast access continuity cache memory within the same processor, the resulting modification would still fail to reach the limitations of claim 1.

Rather, the result would be an arrangement similar to that discussed in the present specification at, for example, page 9, lines 1-6, in which one bit is set for each active flow to indicate if the counter for that flow has already been cleared during the timeout window. This arrangement prevent multiple accesses to memory for the same flow, but requires that a bit be stored in internal memory for every possible flow, thus resulting in an excessive consumption of on-chip memory resources. Such an arrangement would fail to reach the advantages associated with illustrative embodiments of the claimed invention, such as substantially reducing the required number of external memory accesses while also reducing the amount of memory resources that are consumed. See, for example, the present specification at page 3, lines 9-16, and page 9, lines 7-12.

Independent claims 19 and 20 contain limitations similar to those recited in claim 1 and are thus believed allowable for at least the reasons identified above with regard to independent claim 1.

Dependent claims 2-18 are believed allowable for at least the reasons identified above with regard to independent claim 1, from which each depends. Moreover, at least one of these claims defines independently patentable subject matter.

For example, dependent claim 6 includes limitations wherein the continuity check cache has a capacity of M entries and the set of continuity check counters includes N continuity check counters, where M is substantially less than N. The Examiner contends that this limitation is suggested by block 32 in FIG. 3.

Applicant respectfully disagrees and instead notes that FIG. 3 of Park in fact teaches away by instead showing continuity check timer part 32 comprising Timer-1, Timer-2, ..., Timer-N, and continuity check channel registration part 34 comprising Continuity Checking Cell Channel-1, Continuity Checking Cell Channel-2, ..., Continuity Checking Cell Channel-N. See also Park at column 9, lines 23-26 ("continuity clock timer part 32 includes a plurality of timers corresponding respectively to continuity check connections in the continuity check cell channel registration part 34.")

In view of the above, Applicant believes that claims 1-20 are in condition for allowance and request withdrawal of the present rejections and objections.

Respectfully submitted,

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